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TESTING AND VERIFICATION OF (7, 4) HAMMING CODE USING HDL

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ABSTRACT

A communication system mainly comprises of a transmitter section and a receiver section linked through a channel. Such a system is said to be efficient if the data received at the receiver is exactly what was transmitted. But it is a well known fact that, the message transmitted can get distorted due to several disturbances in its path. In order to reduce the occurrence of error in digital communication system, the message signal will be coded using an encoder. At the receiver section, a decoder is used for the purpose of decoding the signal. This project is intended to analyze the encoder and decoder using Hamming code. Hamming code is a linear block code. In the encoder, parity symbols are generated using generator polynomial. Hamming code is capable of correcting all error patterns with a single error or detecting all the error patterns of two or fewer errors. The project proposes encoding algorithm, synthesis and simulation using Verilog HDL. The implementation of Hamming code encoder using Spartan-6 FPGA kit was also done.

I. INTRODUCTION

In telecommunication, a communication system is a collection of communication networks, transmission systems, relay stations etc. A communication system mainly comprises of a transmitter section that transmits the message to be transferred and a receiver section that receives the message. At some cases, there will be transducers prior to the transmitter and after the receiver for the purpose of converting one form of signal to the other. The transmitter and the receiver are interconnected by means of a suitable channel. This system is said to be efficient if the data received at the receiver is exactly what was transmitted. But the message transmitted can get distorted. Now a day; as demand is continuously increasing for development of reliable telecommunication and wireless systems, it is important to detect and correct errors in the information received through communication channels. Therefore error control coding is important in communication system design.

Communication systems are broadly classified into two: Analog Communication systems and Digital Communication systems. Among this, Digital Communication system is the most commonly used one and is also having certain advantages over Analog communication systems. Digital communication provides security to the information signal. It has more immunity to noise and external interference than analog communication system. Digital information can be saved and retrieved when necessary, while it is not possible with analog systems. Digital communication is cheaper than analog communication. The configuring process of digital communication is complex, but is simple as compared to analog communication system.

Digital communication system is a system which makes use of binary 1s and 0s for the transmission and reception. In order to reduce the occurrence of error in a digital communication system, the message signal will be coded using an encoder. At the receiver section, a decoder is used for the purpose of decoding the signal.

The coding concept was introduced for the detection of error in the data. Actually coding theory is the branch of mathematics that is concerned with accurate and efficient transfer of data across noisy channels. The primary goal of coding theory is the encoding of information, easy transmission of encoded messages, fast decoding of received information and correction of errors introduced in the channel. The general block diagram of a digital communication system is as shown in the following block diagram.

The transmitter section consists of source encoder and channel encoder and the receiver section comprises of channel decoder and source decoder connected using a channel. Message sources are the origins of message or input signal. A source encoder is used for the purpose of converting symbols to binary representation.

The output of source encoder is fed to channel encoder. The channel encoder converts messages into code words by adding parity digits for the purpose of error free transmission through the channel. This codeword is then transmitted through the channel. A communication channel is simply referring to the medium by which a signal travels. There are different types of channels according to the type of transmission like optical fibers, coaxial cables or air in case of wireless communication. It is in this phase of communication that most of the errors can occur.

Errors can be of two types - single bit error and burst error. Single bit error can be caused by inverting a single bit and more than one bit inversion can be indicated by burst errors. Noise can get interfered with the message in the channel. The signal that is passed through the communication channel must be effectively captured by a receiver. The codeword transmitted through the channel is first subjected to channel decoding. Channel decoder obtains the transmitted codeword and this is then given to source decoder. The source decoder will give out the transmitted message. Source coding can be done using different methodologies like Huffman coding, Shanon Fano coding and Lempel Ziv coding. Channel coding can be done by Hamming coding, RS coding etc.

In this project, the main focus of the work is on the channel encoding and decoding. Channel coding maps the input message to channel input sequence and also maps the channel output sequence to output data by reducing the effect of channel noise. The most commonly used channel coding techniques are Reed Solomon code and Hamming code which are having importance in real time applications. The main objective of the project is to implement Hamming encoder and decoder. Codes are programmed using Verilog language and are simulated using Xilinx ISE 14.2 simulator. The Xilinx project navigator is used for synthesis. The encoding section was implemented using Spartan-6 FPGA.

A. Linear Block Code (LBC)

In block coding, the binary information sequence is segmented into message blocks of fixed length. Each message block is denoted by 'u' consists of k information digits, with which we have 2^k distinct messages. The channel encoder transforms each message u into a binary n-tuple 'v' with nk where n-tuple v is referred to as the codeword of the message u. There are 2k code words corresponding to 2k distinct messages. A block code of length 'n' and 2k code words is called a linear block code (n,k) if and only if '2k' code words form a k-dimensional subspace of the vector space of all the n-tuples GF(2).

A block code is linear if and only if the modulo-2 sum of two code words is also a code word. The desirable property of a linear block code is that it should have a systematic structure of the code word in which a code word is divided into two parts, the message part and the redundant checking part. A linear systematic (n, k) code can be specified by a (k × n) matrix G, the generator matrix. The code word can be generated by multiplying the message with the generator matrix. The generator matrix G consists of k linearly independent code vectors; such that every code word 'v' can be generated using the linear combination of these k rows. At the same time there is a parity check matrix at the receiver side for the purpose of detection of the errors. For any (k × n) matrix G, there exist an ((n-k) × n) matrix H with (n-k) linearly independent rows such that any vector in the row space of G is orthogonal to the rows of H and any vector that is orthogonal to the rows of H is in the row space of G.

B. Hamming Code

Hamming codes are a family of binary linear error-correcting codes, which was invented by Richard Hamming in 1950. Hamming codes can detect up to two-bit errors and correct one-bit error without detection of uncorrected errors. Hamming codes are perfect codes, which can achieve the highest possible rate for codes with their block length and minimum distance of three. Hamming code is capable of correcting all error patterns with a single error or detecting all the error patterns of two or fewer errors. For a code to be called as Hamming code, it should satisfy the following conditions:

Number of parity bits, $m = n-k$

Length of code word, $n = 2^m-1$

Length of message, $k = 2^m-m-1$

Hamming codes are having a wide variety of applications in the field of digital communication. It is used in modern communication systems such as digital mobile radio (DMR) and in Satellite communication hardware. Hamming codes also find its application in the error correction of D-RAM memory chip in low power with high performance.

The encoding section comprises of a part to calculate the parity bits to be concatenated with the message bits to obtain the codeword. At the decoding side, syndrome is calculated from the received codeword. It is according to this syndrome that error detection and correction are made possible. If syndrome is 0, this implies that there is no error occurred while transmitting through the channel. Otherwise, according to the syndrome vector, corresponding single bit error pattern is obtained by which the occurred error can be corrected.

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II. METHODOLOGY

Encoding and decoding for (7, 4) Hamming code is performed. For a (7, 4) hamming code, there are 4 message bits. The length of the code word is 7 bits. Thus there are 3 parity digits to be added with the message bits. There will be 3 bits for the syndrome.

C. Hamming Encoder

In order to get the code word there should be a generator matrix. A generator matrix is obtained by combining parity matrix (P) and identity matrix (I). In this case, the parity matrix is of size (4   3) and the identity matrix of size (4   4). The generator matrix that is used in this work is given as,
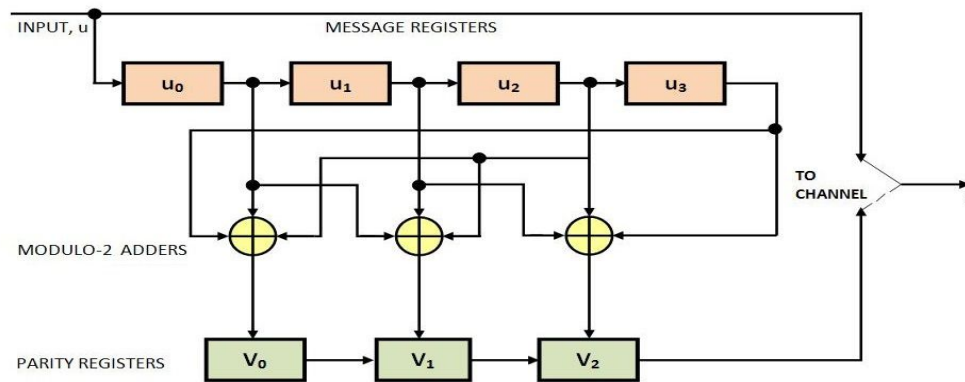
$$G = \begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & 1 \end{bmatrix}$$

The code word is generated by multiplying message with generator matrix. According to this, the inputs to the Modulo-2 adder varies as,

$V_0 = u_0 + u_2 + u_3$
$V_1 = u_0 + u_1 + u_2$
$V_2 = u_1 + u_2 + u_3$
$V_3 = u_0$
$V_4 = u_1$
$V_5 = u_2$
$V_6 = u_3$

The block diagram for the above given generator matrix is as in figure. The inputs to the adders are according to the 1's and 0's in 'G'. After performing modulo-2 addition parity bits are obtained. After transmitting the parity digits, the channel switches to input line and the remaining 4 bits are transmitted. All possible 4-bit messages and their corresponding Hamming codes are given in the table.

Figure:

Block diagram of (7, 4) Hamming Encoder

Table 1. (7, 4) Hamming Codes

Sl No.	Message (u0 u1 u2 u3)	Hamming Code (v0 v1 v2 v3 v4 v5 v6)	Sl No.	Message (u0 u1 u2 u3)	Hamming Code (v0 v1 v2 v3 v4 v5 v6)
1.	0 0 0 0	0 0 0 0 0 0 0	9.	1 0 0 0	1 1 0 1 0 0 0
2.	0 0 0 1	1 0 1 0 0 0 1	10.	1 0 0 1	0 1 1 1 0 0 1
3.	0 0 1 0	1 1 1 0 0 1 0	11.	1 0 1 0	0 0 1 1 0 1 0
4.	0 0 1 1	0 1 0 0 0 1 1	12.	1 0 1 1	1 0 0 1 0 1 1
5.	0 1 0 0	0 1 1 0 1 0 0	13.	1 1 0 0	1 0 1 1 1 0 0
6.	0 1 0 1	1 1 0 0 1 0 1	14.	1 1 0 1	0 0 0 1 1 0 1
7.	0 1 1 0	1 0 0 0 1 1 0	15.	1 1 1 0	0 1 0 1 1 1 0
8.	0 1 1 1	0 0 1 0 1 1 1	16.	1 1 1 1	1 1 1 1 1 1 1

D. **Hamming Decoder**

At the decoder side, syndrome is calculated from the received vector. For this purpose, parity check matrix or H- matrix is introduced. It is obtained by combining identity matrix (I) and transpose of parity matrix (P^T). In this case, identity matrix is having size (3×3) and parity matrix is having the size (3×4).The H-matrix for the given generator matrix is as follows,

$$H = \begin{bmatrix} 1 & 0 & 0 & 1 & 0 & 1 & 1 \\ 0 & 1 & 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 1 & 1 \end{bmatrix}$$

Form this syndrome can be obtained as, $S = R*H^T$, where H^T represents transpose of matrix H. Thus syndrome can be calculated by the following equations.
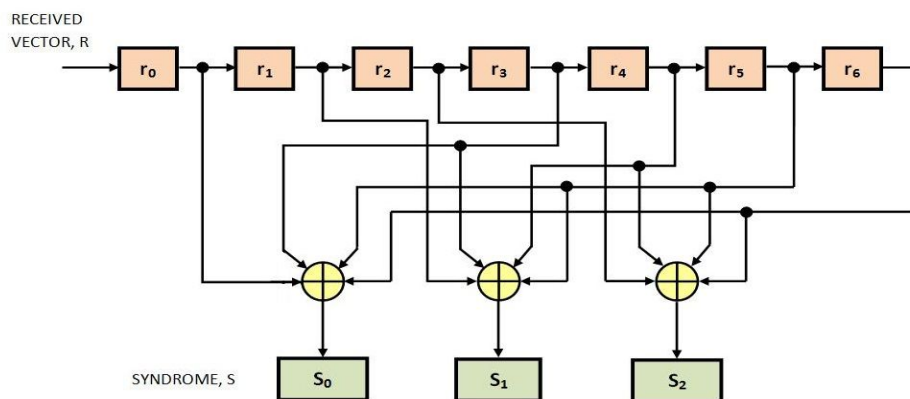$S_0 = r_0 + r_3 + r_5 + r_6$
$S_1 = r_1 + r_3 + r_4 + r_5$
$S_2 = r_2 + r_4 + r_5 + r_6$
According to this the syndrome is computed using the following block diagram. Modulo-2 adders are used to obtain the syndrome.
Figure:

Block diagram for obtaining syndrome

The single bit error pattern corresponding to each syndrome is as given in the following table. If syndrome is 0, it implies that no error is occurred to the codeword while transmitting through the channel. If it is not equal to 0, then it is concluded that some error has been occurred and if it is a single bit error, it can be nullified by performing modulo-2 addition between received vector and error pattern.

Table 1. (7, 4) Hamming Codes

Syndrome			Error Pattern						
S_0	S_1	S_2	r_0	r_1	r_2	r_3	r_4	r_5	r_6
0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0
0	0	1	0	0	1	0	0	0	0
1	1	0	0	0	0	1	0	0	0
0	1	1	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1

III. SOFTWARE DETAILS

E. *HDL language and HDL programming*

Most commonly used HDL language by Integrated Circuit Designers is Verilog HDL. It is also used in electronic design applications in analog and mixed analog signals such as FPGA. VHDL can also used as parallel programming language. The initial version of HDL had a lot of data types than that existing today. It is commonly used to write text models that describe logic circuit. Part of the program is processed by a synthesizer program, only if it is a part of logic design. Simulation program is used to simulate models to represent the logic circuits that interface to the design. This group of simulation models are called test bench. In each HDL transaction event is added to queue. VHDL is not case sensitive. To represent higher operations Boolean Operations are included. HDL allows the design to be simulated earlier during the design in order to correct errors. Designs described in HDL are technology-independent, easy to design and debug. These are usually more readable than schematics, particularly for large circuits.The language also defines constructs that can be used to control the input and output of simulation. The very important advantage of VHDL is that it also allows the description of concurrent system.

F. *Xilinx 14.2 Simulation Software*

Xilinx ISE is a software tool produced by Xilinx for synthesizing HDL languages. It gives a platform to for user to synthesize or compile their designs, examine RTL diagram etc. Xilinx ISE is design environment for FPGA products from ISE. It is primarily used for circuit synthesis and design. System level testing is done by ModelSim or ISIM logic simulator. Vivado Design is served as the additional feature for chip level design. Primary user interface is ISE project navigator. It has Sources, Workplace, Transcript, Processes etc. The processes hierarchy describes the operations that the ISE and displayed as Tree structure. Hierarchy include design function, and other utilities. Xilinx patented algorithms for synthesis allow designs to run up faster. Due to increasing complexity of FPGA, including memory blocks and I/O blocks were developed to separate unread module into slices. In FPGA based implementation Xilinx has been an Instrumental design.

IV. HARDWARE DETAILS

G. *Sparatn-6 FPGA*

The Spartan-6 family of Field-Programmable Gate Arrays (FPGAs) is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. Spartan-6 devices offer industry-leading connectivity features such as high logic-to-pin ratios, small form-factor packaging, Micro Blaze soft processor, and a diverse number of supported I/O protocols. Ideally it is suited for a range of advanced bridging applications found in consumer, automotive infotainment, and industrial automation. FPGAs avoid the high initial cost, thelengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary. Spartan-6 FPGA is available in various speed grades, with the highest performance. The DC and AC electrical parameters of the Automotive Spartan-6 FPGAs and Defense grade Spartan-6Q FPGAs devices are equivalent to the commercial specifications. Up to 8 low power 3.2Gb/s serial transceivers, 800Mb/s DDR3 with integrated memory controller are incorporated for increased system performance. Total Power Reduction is made possible by 1.2V core voltage or 1.0V core voltage option.

V. RESULTS AND DISCUSSIONS

The Verilog program for Hamming encoder was simulated using the Xilinx software and the result is obtained in ModelSim. By using a test bench program all the messages that are possible in 4-bit combination are obtained. Also the respective code word for particular message was also obtained. Figure shows the simulation result for this case. In this case for all the possible 4-bit combinations, there is a code word generated, which is of length 7 bits. Also the program for obtaining single codeword corresponding to any 4-bit message input combination was also simulated. The encoding section is implemented using Spartan-6 FPGA and the outputs corresponding to each message was obtained. Inputs were given using switches provided in the kit and the outputs were verified by observing the LED lights.
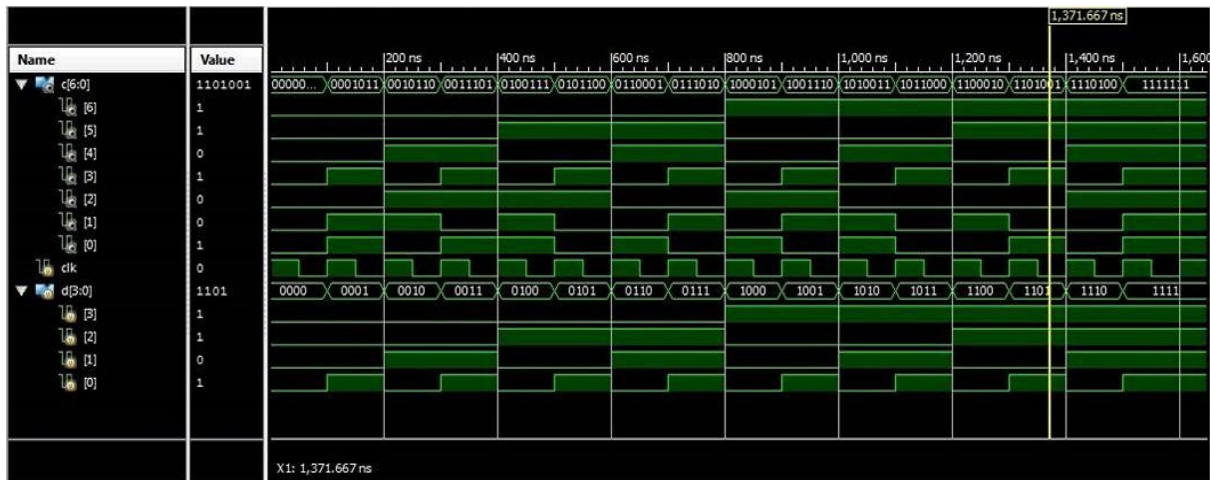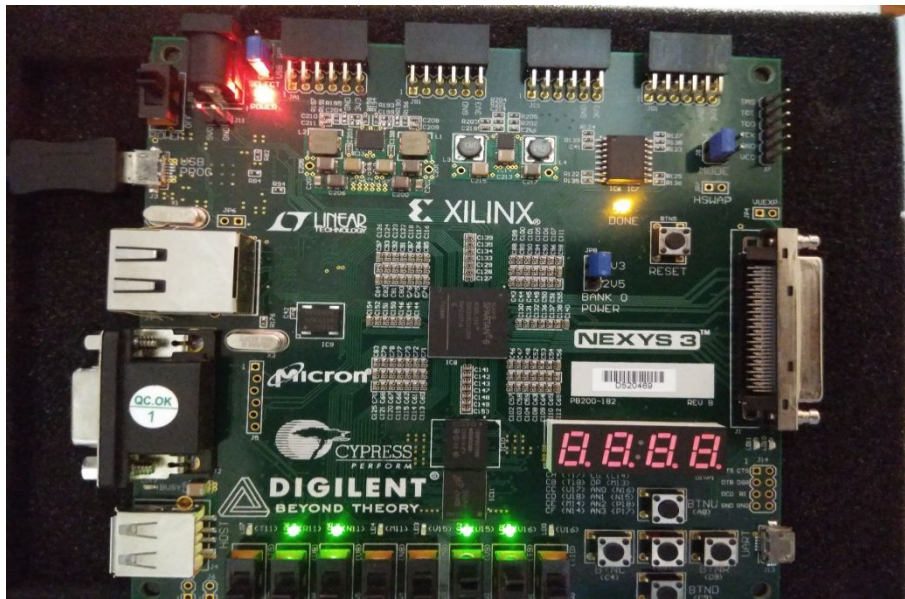
Figure:

Simulation result for (7, 4) Hamming Encoder with codewords for all 4-bit messages

Figure:

Implementation of (7, 4) Hamming Encoder in Spartan-6 FPGA

VI. CONCLUSION

Hamming code is a channel code which is easy to implement and is less complicated. Hamming codes are capable of detecting 2 bit errors and can correct the single bit errors that had occurred while transmitting through the channel. It can't detect more than 2 bits and correct more than 1 bit. This is identified as a drawback of this channel code. By considering its easiness to use and applications in digital communication, Hamming codes are much more important.

VII.   ACKNOWLEDGEMENTS

VIII. REFERENCES

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